What is claimed is:

1. A semiconductor memory device having a uniform bit line sensing margin time independent on an external voltage variation, comprising:

a memory cell coupled to a bit line and a word line;

an amplification means for amplifying an electric potential of the bit line;

a first control signal generating means to which an external voltage is supplied for activating the word line; and

a second control signal generating means to which a core voltage is supplied for controlling an execution of the amplification means by receiving the first control signal.

2. The semiconductor memory device as recited in claim 1, wherein the second control signal generating means includes a delay circuit to which the core voltage is supplied for performing a delay operation of the first control signal by a delay as much as the sensing margin time of the amplification means.

3. The semiconductor memory device as recited in claim 1, further comprising:

a level shifting means to which the external voltage is supplied for performing a level shifting operation of a voltage level of the second control signal.

4. An operating method of a semiconductor memory device having a memory cell coupled to a word line and a bit line, comprising the steps of:

a) generating a first control signal by supplying an external voltage in order to activate the word line; and

b) generating a second control signal by supplying a core voltage in order to amplifying an electric potential of the bit line by receiving the first control signal.

5. The method as recited in claim 4, wherein said step b) includes the step of:

b1) performing a delay operation of the first control signal by a delay as much as the sensing margin time,

wherein the delay operation is executed by supplying the core voltage.

6. The method as recited in claim 4, further comprising the step of:

c) performing a level shifting operation of a power level of the second control signal,

wherein the level shifting operation is executed by supplying the external voltage.

7. A semiconductor memory device, comprising:

a memory cell coupled to a bit line and a word line;

an amplification means which is coupled to the bit line for amplifying an electric potential of the bit line;

an active signal generating means to which an external voltage is supplied for generating an active signal that is activated during an active operation and inactivated during a precharge operation;

a word line timing control means to which the external voltage is supplied for generating a first control signal in order to activate a word line by receiving the active signal;

a row decoder/driver for activating a chosen word line with responding to the first control signal;

a sensing timing control means to which a core voltage is supplied for generating a second control signal in order to control the amplification means by receiving the first control signal; and

a sense amplifier control means for generating an enable signal of the amplification means with responding to the second control signal.

8. The semiconductor memory device as recited in claim 7, further including:

a level shifting means to which the external voltage is supplied for performing a level shifting operation of a power level of the second control signal and outputting the level shifted signal to the sense amplifier control means,

wherein the external voltage is supplied to the sense amplifier control means.

9. The semiconductor memory device as recited in claim 7,

wherein the amplification means includes:

an amplifier for amplifying a signal of the bit line; and

a supply voltage generating means for generating a supply voltage of the amplifier with responding to the enable signal.